(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 326 940 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **89101330.2**

(51) Int. Cl.⁴: **H03L 7/10**

(22) Date of filing: **26.01.89**

(30) Priority: **03.02.88 US 151870**

(43) Date of publication of application:
09.08.89 Bulletin 89/32

(84) Designated Contracting States:
DE FR GB IT

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(54) A phase locked loop having a fast lock current reduction and clamping circuit.

(57) There is disclosed a circuit (60) responsive to control signals applied thereto for alternatively sourcing and sinking current at an output which includes a first controlled current source (48) responsive to selective ones of the control signals for sourcing a current of a predetermined magnitude to the output of the circuit; a second controlled current source (50) responsive to other selective ones of the control signals for sinking a current of a predetermined magnitude from the output of the circuit; and a disabling circuit (42, 44) for respectively disabling said first and second controlled current sources whenever the voltage potential at the output of the circuit becomes greater or less than a predetermined value respectively.

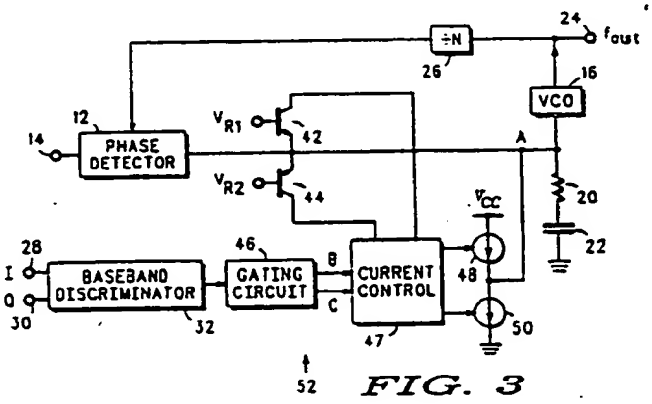

FIG. 3

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A PHASE LOCKED LOOP HAVING A FAST LOCK CURRENT REDUCTION AND CLAMPING CIRCUIT

Background of the Invention

The present invention relates to phase locked loops (PLL) and, more particularly, to means for reducing the current during fast lock up conditions when the PLL is out of the lock up range of the voltage controlled oscillator (VCO) of the PLL.

In a PLL system it is often desirable to speed up the lock up time for acquiring an input signal. One of the most common methods of providing fast lock up is to increase the loop filter charging current when the PLL is out of lock. However, if the input signal is out of the lock up range of the VCO, the phase detector of some, if not all, prior art PLL's will pull the control voltage all the way to one end of its range and the high charging current will continue to charge the loop filter at the beat note frequency (the frequency difference between the input signal and the VCO output). In battery operated equipment this represents unwanted current drain, and in radio receivers the pulsating current may couple into the audio circuits through common impedances which is undesirable.

Hence, a need exist for a means for reducing the fast lock current drain whenever the PLL is at either end of the lock up range.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an improved PLL.

Another object of the present invention is to provide a means for reducing the charging current in a PLL when out of the lock range thereof.

In accordance with a first aspect of the present invention, there is provided a circuit responsive to control signals applied thereto for alternatively sourcing and sinking current at an output which includes a first controlled current source responsive to selective ones of the control signals for sourcing a current of a predetermined magnitude to the output of the circuit; a second controlled current source responsive to other selective ones of the control signals for sinking a current of a predetermined magnitude from the output of the circuit; and disabling circuit for respectively disabling said first and second controlled current sources whenever the voltage potential at the output of the circuit becomes greater or less than a predetermined value respectively.

In accordance with a second aspect of the present invention there is provided a phase or quadrature locked loop including a low pass filter and means for generating quadrature beat notes whenever the phase locked loop is out of lock and circuit means for generating alternating control signals, wherein the improvement comprises a circuit for providing fast lock pull up and pull down currents to the low pass filter when the phase locked loop is out of lock and for reducing such currents when the control voltage developed by the low pass filter becomes either greater or less than a predetermined value, the circuit including:

a first controlled current source responsive to selective ones of the control signals for sourcing a current of a predetermined magnitude to the output of the circuit;

a second controlled current source responsive to other selective ones of the control signals for sinking a current of a predetermined magnitude from the output of the circuit; and

disabling means for respectively disabling said first and second controlled current sources whenever the voltage potential at the output of the circuit becomes greater or less than a predetermined value respectively.

Brief Description of the Drawings

Fig. 1 is partial block and schematic diagram illustrating a prior art PLL having improved lock-in circuitry;

Fig. 2 is a simplified partial block and schematic diagram illustrating a PLL of the present invention;

Fig. 3 is a simplified partial block and schematic diagram illustrating the PLL of the preferred embodiment; and

Fig. 4 is a detailed schematic illustrating the fast lock current control circuit of the present invention.

Detailed Description of the Preferred Embodiment

Turning to Fig. 1 there is illustrated a simplified schematic of a prior art PLL system 10. PLL 10 is fully described in U. S. Patent No. 4,377,728. PLL 10 includes phase detector 12 which receives a signal input at terminal 14 and generates an error beat note signal whenever the output frequency of VCO 16 differs from the frequency of the signal input. The error signal is coupled through gate 18 to a low pass filter comprising series connected

resistor 20 and capacitor 22. A dc control voltage is extracted from the error signal and is applied to the input of VCO 16 which varies the output frequency, f_{out}, of the oscillator provided at output 24. A divide by N circuit 26, where N is any positive number, may be included for dividing the output frequency of VCO 16 before it is applied to a second input of phase detector 12. In phase (I) and quadrature related phase (Q) signals derived from the input signal are applied to inputs 28 and 30 of baseband discriminator 32 the output of which controls the operation of gate 18.

Whenever PLL 10 is locked to the frequency of the signal input, i.e., an IF stereo composite signal of an AM stereo receiver, gate circuit 18 is closed by baseband discriminator 32. This allows the output of phase detector 12 to be coupled directly to the low pass filter comprising resistor 20 and capacitor 22. Hence, a dc control voltage is supplied to the input of VCO 16 to maintain PLL 10 phase locked to the input signal as is well understood. When, the VCO frequency is not tuned closely enough to the incoming stereo input signal PLL 10 will be out of lock. In this condition in-phase and quadrature phase beat notes are produced and supplied to baseband discriminator 32 which provides a controlling signal to gate 18 to provide fast pull in of VCO 16. Fast pull in and locking occurs by a single polarity current being supplied from the gate to charge or discharge capacitor 22 during fast lock. Thus, baseband discriminator 32 determines in which direction to pull the VCO frequency to acquire phase lock by producing the correct output signal and applying the same through gate 18. Hence, during fast lock conditions, the current in the phase detector is increased during appropriate half cycles. Once the VCO reaches a frequency at which lock up occurs, the beat notes will disappear and gate 18 is again closed. For a detailed explanation of the above operation reference is made to the aforementioned '728 US Patent, the teachings of which are incorporated herein by reference made thereto.

Turning now to the remaining Figures there is shown an improved PLL 40 in Fig. 2 for providing fast lock current. It is noted that components of Figs. 2 and 3 corresponding to like components of Fig. 1 are designated by the same reference numerals. As illustrated, the output of phase detector 12 of PLL 40 is directly coupled to the low pass filter and to the control input of VCO 16. PLL 40 provides the current for fast lock in parallel with phase detector 12. In this embodiment either current source 48 or current sink 50 will be turned on by gating circuit 46, which is coupled to the output of baseband discriminator 32, to pull VCO 16 in the proper direction to acquire lock. The interconnection between the series connected current sources 48 and 50 is coupled to the low pass filter at node A to provide fast current charging or discharging of capacitor 22 as will be explained.

Clamping transistors 42 and 44 are utilized to limit the excursion of the control voltage at node A when PLL 40 is out of lock in order to keep the control voltage supplied to VCO 16 within the operating range of the VCO. This prevents capacitor 22 from being charged or discharged to outside the useful control range. Hence, as soon as the voltage developed across capacitor 22 and resistor 20 drops below a V_{BE} of V_{R1} transistor 42 turns on to limit the voltage to the input of VCO 16 to V_{R1}-V_{BE}. Likewise when the voltage at node A increases by a V_{BE} above V_{R2} transistor 44 is turned on to clamp node A at this potential. Thus, VCO 16 is maintained within its controllable range.

The fast lock current is controlled by baseband discriminator 32. Baseband discriminator 32 via gating circuit 46 turns on either pull up current source 48 or pull down current source 50 at the beat note pulse rate, producing a square wave of current either in or out of phase with the quadrature signal.

An undesirable effect occurs when the incoming signal to the phase detector is of a frequency outside of the controllable range of VCO 16. The voltage will be driven to the point where one of the clamping transistors are turned on. The particular clamping transistor will conduct almost all of the current supplied by the fast lock circuit for as long as the out of lock range condition exists. This wasted current is very undesirable if the circuit is battery powered. It also has a possibility (being of a pulsating nature) of coupling into other circuits through common impedances. In radio equipment this could result in an audible tone being heard at the audio output.

As shown in the circuit of Fig. 3 of the present invention clamping transistors 42 and 44 are used to reduce the amplitude of the fast lock current supplied by current source 48 or current sink 50 whenever the control voltage to VCO 16 turns on one of the clamps. As illustrated the collector of transistor 42 and the collector of transistor 44 are coupled to current amplitude control circuit 47. Control circuit 47 has inputs at nodes B and C to receive the gating control signals from gating circuit 46 to in turn on one of the current sources 48 or 50 as previously described.

In operation, as the control voltage at node A drops a diode voltage below V_{R1} clamp transistor 42 turns on to reduce the fast lock current sourced by current sink 50. Similarly, when the control voltage to VCO 16 appearing at node A becomes greater than a diode voltage above V_{R2} transistor 44 is turned on to reduce the fast lock current supplied by current source 48.

Turning now to Fig. 4 fast lock current and clamping circuit 60 of the present invention is shown in detail. Clamping transistors 42 and 44 each of which have their emitters coupled to the base of buffer transistor 64 and to input terminal 62, which comes from the output of phase detector 12 provide clamping of the VCO control voltage in the same manner as described above. In this embodiment, the bases of the two clamping transistors are coupled to a common reference potential at terminal 45. Emitter follower buffer transistor 64 supplies the control voltage at its emitter to VCO 16 which is connected thereto at terminal 66 while the collector of the transistor is coupled to power supply conductor 68 at which the operating potential Vcc is supplied. Multiple collector transistor 70 having its emitter coupled to power supply conductor 68 functions as a current mirror with its base and one collector being interconnected to the collector of clamping transistor 42. The output of circuit 60 is provided to node A to one end of resistor 20, the other end of which is connected to capacitor 22 at terminal 74.

Pull up controlled current source 48 is realized by a pair of current mirror circuits 76 and 78 while pull down controlled current source 50 is realized by a single current mirror circuit 80 which is substantially identical to current mirror circuit 76. Current mirror circuits 76, 78 and 80 are generally well understood to those skilled in the art. Current mirror circuit 76 is comprised of transistors 82 and 84 the bases of which are connected in common to the emitter of transistor 90. The emitters of transistors 82 and 84 are respectively coupled via resistors 86 and 88 to a second power supply conductor to which is supplied ground reference potential. The collector of transistor 82 is connected to the base of transistor 90, the collector of the latter of which is connected to Vcc. As understood, the collector of transistor 82 may be directly connected to its base to form a diode although the present connection via the base-emitter of transistor 90 provides the same function. The output of current mirror circuit 76 is provided at the collector of transistor 84 and is coupled to the input of current mirror circuit 78 at the collector of transistor 92. The base of transistor 92 is connected to the base of transistor 94 with the emitters of the two being coupled to power supply conductor 68. The output of current source 48 corresponds to the collector of transistor 94 and is coupled to node A. Transistor 96 having its base-emitter coupled between the base and collector of transistor 92 and its collector connected to ground potential functions similarly to transistor 90 to provide base current compensation as is understood. Current mirror circuit 80 is identical to current mirror circuit 76 and includes transistors 98, 100 having commonly connected bases and emitters respectively coupled via resistors 102 and 104 to ground reference potential and base compensation transistor 106. The output of current mirror circuit 80 is taken at the collector of transistor 100 and is coupled to node A. The inputs to current mirror circuits 76 and 80 (the collectors of transistors 82 and 98) are coupled to terminals 108 and 112 via control lines 110 and 114. These input reference currents are supplied from gating circuit 46, shown in Fig. 3.

Current mirror circuits 76 and 80 are enabled or disabled by the state of conduction of control transistors 116 and 120 respectively. Transistor 116 which has its base coupled to the collector of clamping transistor 44 and its collector-emitter conduction path coupled between control line 110 and ground is controlled by the operation of transistor 44 being biased accordingly via resistor 118. Similarly, transistor 120 is biased in accordance with the conduction of transistor 42 via the second collector of transistor 70 being coupled both to the base of the transistor and via resistor 122 to ground reference potential. The collector-emitter conduction path of transistor 120 is coupled between control line 114 and ground reference potential.

Circuit 60 is controlled by baseband discriminator 32 and gating circuit 46 to provide fast lock current whenever PLL 40 is out of lock. As will be described later, when out of lock either pull up current source 48 or pull down current source 50 is turned on at the beat note pulse rate by baseband discriminator 32 to thereby produce a square wave of current either in or out of phase with the quadrature signal. When fast lock circuit 60 is enabled, baseband discriminator 32 via gating circuit 46 supplies reference current pulses on one of the two control lines 110 or 114 to in turn enable one or the other of current sources 48 or 50.

For example, if control line 110 goes high, current mirror circuit 76 is rendered operative as transistor or diode means 82 is turned on which also turns on transistor 84. As transistor 84 is turned on current is pulled from transistor 92 which turns on transistor 94. Pull up fast lock current is thus sourced from the collector of transistor 94 to node A to charge capacitor 22. Current gain may be achieved by ratioing resistors 86 and 88 and/or emitter area ratioing the emitter areas of transistors 92 and 94. Likewise, if control line 114 is high transistor or diode means 98 is turned on thereby turning on transistor 100. Transistor 100 will then sink current from node A to provide fast lock current discharge of capacitor 22. Again by making resistor 102 larger than resistor 104 current gain through current mirror circuit 80 may be realized to provide sufficiently large fast lock discharging current.

To prevent the charging and discharging of capacitor 22 from driving the control voltage to one end of its range during fast lock and for reducing the fast lock current drain either clamping transistor 42 or 44 is turned on to disable respective current source 50 or 48. Hence, if the voltage potential at the base of transistor 64 increases by one V_{BE} above V_R transistor 44 turns on. Thus, the control voltage is prevented from rising further while at the same time transistor 116 is turned on, turning off both current mirror circuits 76 and 78 and turning off the fast lock pull up current. Similarly, if the voltage at the base of transistor 64 falls one V_{BE} below V_R transistor 42 is turned on to clamp the control voltage to this value while transistor 70 is also turned on which turns on transistor 120. Current mirror circuit 80 is thus disabled which turns off the fast lock pull down current.

Hence, what has been described above is a novel fast lock current and clamping circuit for providing fast lock current pull up and pull down to charge and discharge the capacitor in the loop filter of a PLL system while preventing the control voltage thereof form being pulled to one end of its range. The novel circuit also reduces the fast lock current as the control voltage reaches a predetermined value in either direction.

Claims

1. Circuit (60) responsive to control signals applied thereto for alternatively sourcing and sinking current at an output, comprising:
a first controlled current source (48) responsive to selective ones of the control signals for sourcing a current of a predetermined magnitude to the output of the circuit;
a second controlled current source (50) responsive to other selective ones of the control signals for sinking a current of a predetermined magnitude from the output of the circuit; and
disabling means (42, 44) for respectively disabling said first and second controlled current sources whenever the voltage potential at the output of the circuit becomes greater or less than a predetermined value respectively.

2. The circuit of claim 1 wherein said first controlled current source includes:
a first current mirror circuit (76) having an input to which said selective ones of the control signals are applied and an output;
a second current mirror circuit (78) having an input coupled to said output of said first current mirror circuit and an output coupled to the output of the circuit for sourcing the current thereto; and
a first transistor (116) having its collector-emitter conduction path coupled in parallel to said input of said first current mirror circuit which is responsive to a first disable signal supplied from said disabling means to the base thereof for rendering said first and second current mirror circuits disabled.

3. The circuit of claim 1 or 2 wherein said second controlled current source includes:
a third current mirror circuit (80) having an input to which said other selective ones of said control signals are applied, and an output coupled to the output of the circuit; and
a second transistor (120) having its collector-emitter conduction path coupled in parallel to said input of said third current mirror circuit which is responsive to a second disable signal supplied from said disabling means to the base thereof for rendering said third current mirror circuit disabled.

4. The circuit of claim 2 and 3 wherein said disabling 15 means includes:
a third transistor (44) having a base, a collector and an emitter, said base being coupled to a terminal to which a reference potential is supplied, said emitter being coupled to the output of the circuit and said collector being coupled to said base of said first transistor;
a fourth transistor (42) having a base, a collector and an emitter, said base being coupled to a terminal to which a reference potential is supplied, said emitter being coupled to the output of the circuit; and
a fourth current mirror circuit (70) having an input coupled to said collector of said fourth transistor and an output coupled to said base of said second transistor.

5. The circuit of claim 4 wherein said bases of said third and fourth transistors are connected together to a terminal at which is supplied a single reference potential.

6. A phase locked loop including the circuit of claim 5 and comprising a low pass filter to which the output of the circuit is connected thereto.

7. A phase or quadrature locked loop including a low pass filter and means for generating quadrature beat notes whenever the phase locked loop is out of lock and circuit means for generating alternating control signals, wherein the improvement comprises a circuit (60) for providing fast lock pull up and pull down currents to the low pass filter when the phase locked loop is out of lock and for reducing such currents when the control voltage developed by the low pass filter becomes either greater or less than a predetermined value, the circuit including:
a first controlled current source (48) responsive to selective ones of the control signals for sourcing a current of a predetermined magnitude to the output of the circuit;
a second controlled current source (50) responsive to other selective ones of the control signals for

sinking a current of a predetermined magnitude from the output of the circuit; and

disabling means (42, 44) for respectively disabling said first and second controlled current sources whenever the voltage potential at the output of the circuit becomes greater or less than a predetermined value respectively.

8. A phase or quadrature locked loop of claim 7 wherein said first controlled current source includes:

a first current mirror circuit (76) having an input to which said selective ones of the control signals are applied and an output;

a second current mirror circuit (78) having an input coupled to said output of said first current mirror circuit and an output coupled to the output of the circuit for sourcing the current thereto; and

a first transistor (116) having its collectoremitter conduction path coupled in parallel to said input of said first current mirror circuit which is responsive to a first disable signal supplied from said disabling means to the base thereof for rendering said first and second current mirror circuits disabled.

9. A phase or quadrature locked loop of claim 8 wherein said second controlled current source includes:

a third current mirror circuit (80) having an input to which said other selective ones of said control signals are applied, and an output coupled to the output of the circuit; and

a second transistor (120) having its collector-emitter conduction path coupled in parallel to said input of said third current mirror circuit which is responsive to a second disable signal supplied from said disabling means to the base thereof for rendering said third current mirror circuit disabled.

10. A phase or quadrature locked loop of claim 9 wherein said disabling means includes:

a third transistor (44) having a base, a collector and an emitter, said base being coupled to a terminal to which a reference potential is supplied, said emitter being coupled to the output of the circuit and said collector being coupled to said base of said first transistor;

a fourth transistor (42) having a base, a collector and an emitter, said base being coupled to said terminal, said emitter being coupled to the output of the circuit; and

a fifth transistor (70) having a base, first and second collectors and an emitter, said base being coupled both to said first collector and said collector of said fourth transistor, said second collector being coupled to said base of said second transistor and said emitter being coupled to a power supply conductor.

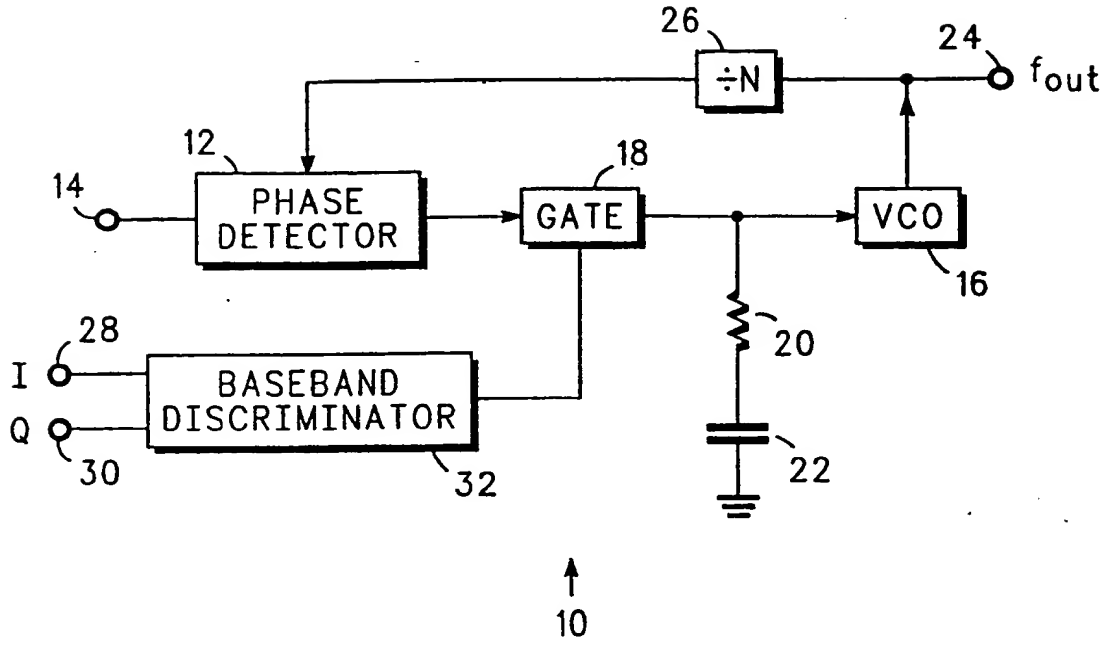
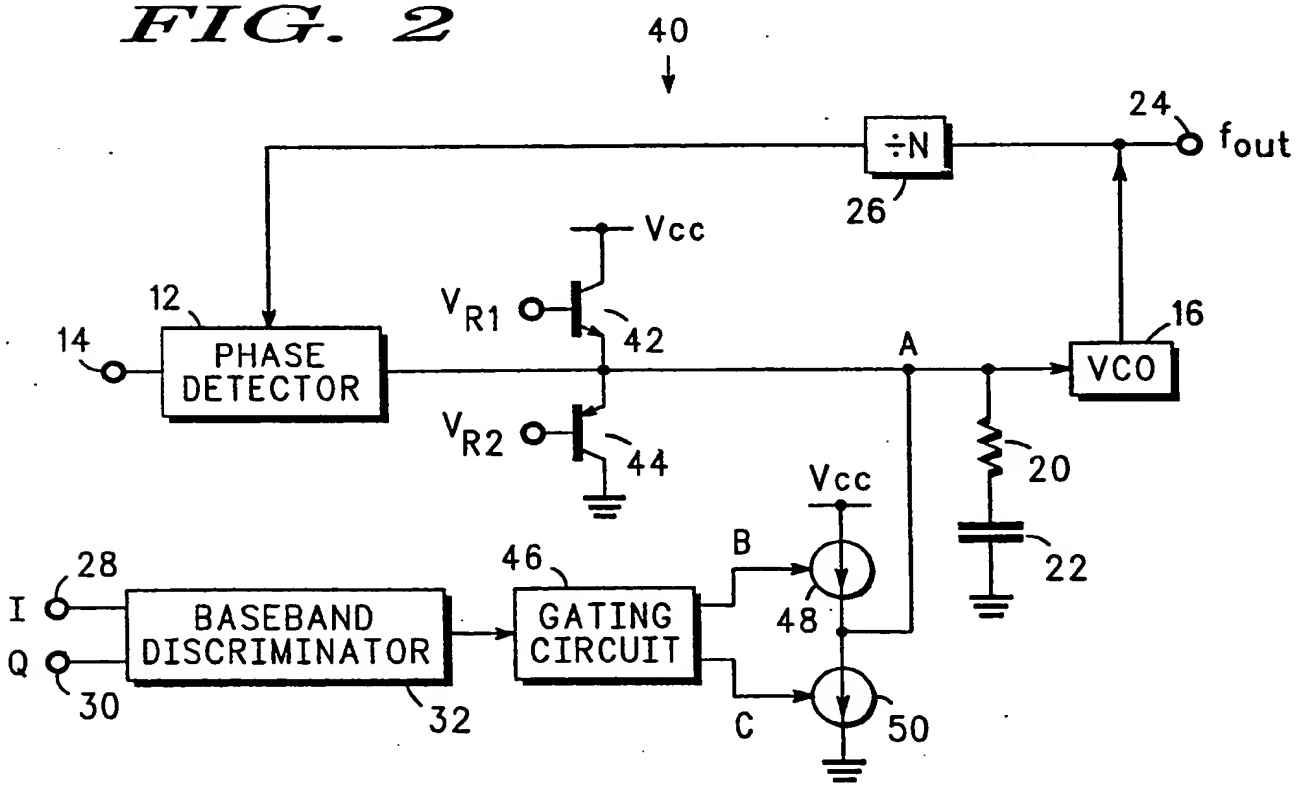


FIG. 1
-PRIOR ART-

FIG. 2



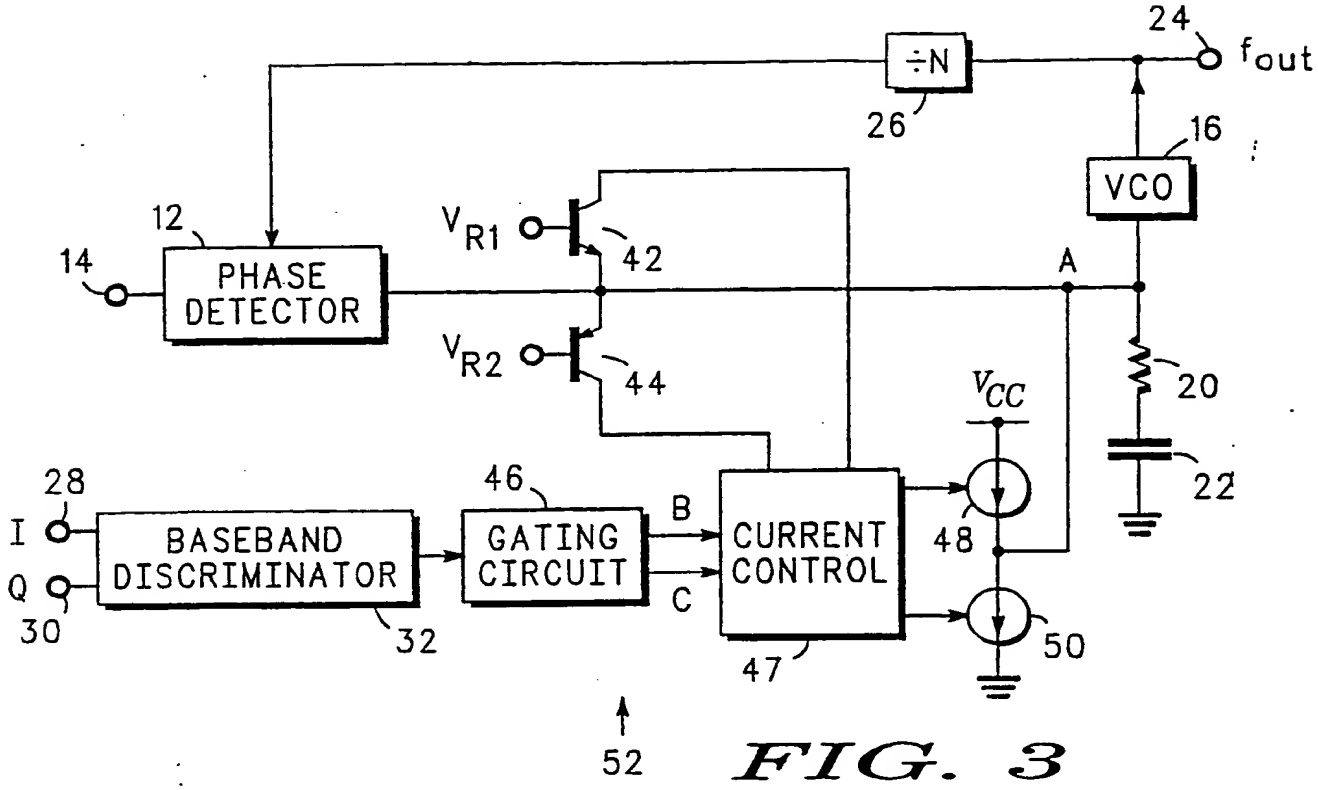
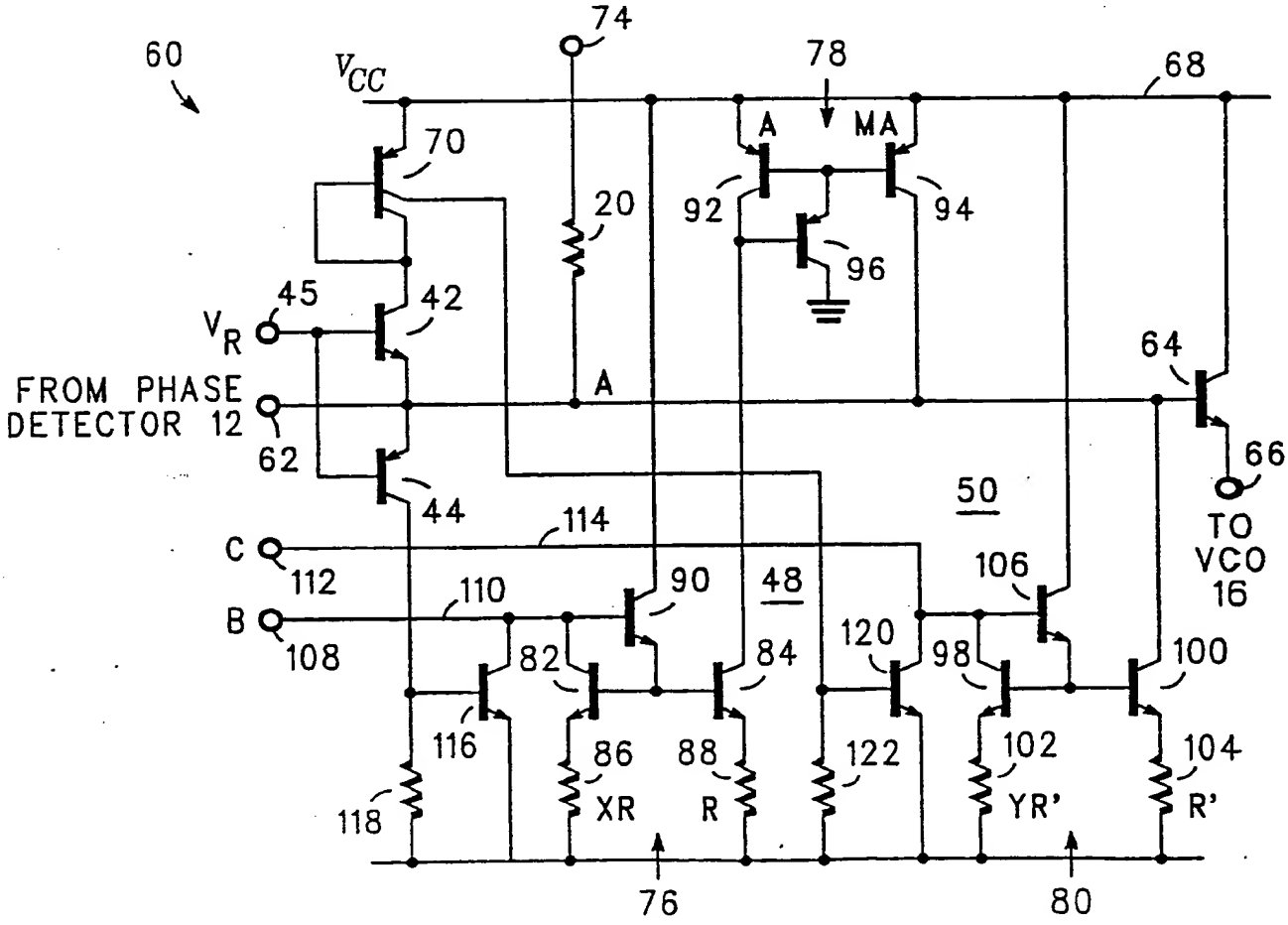


FIG. 3

FIG. 4



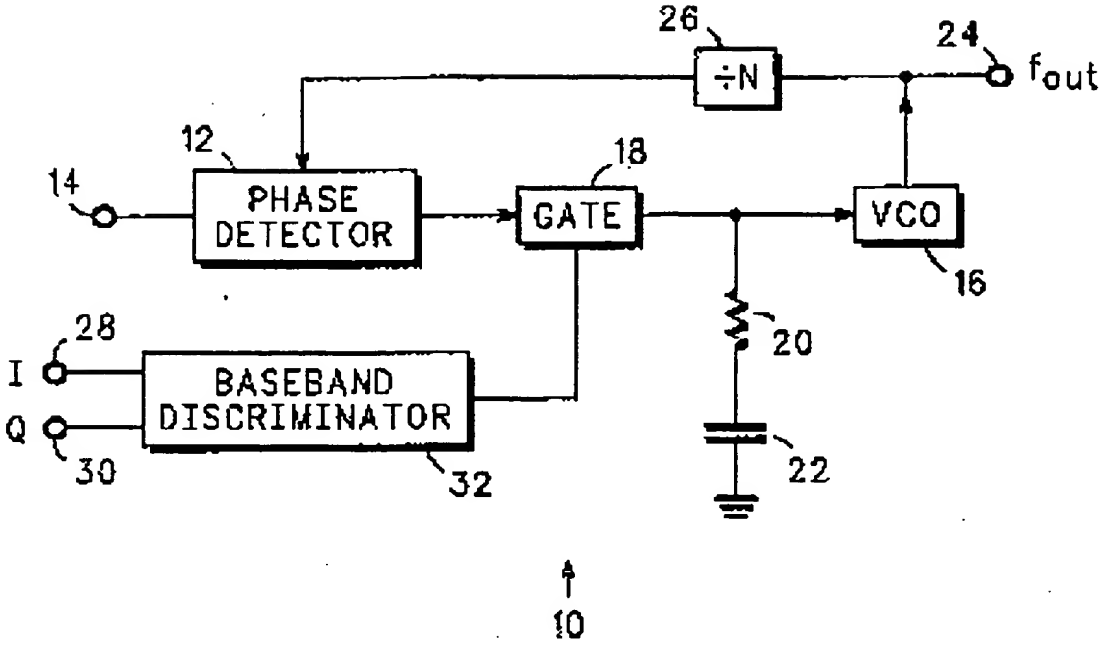
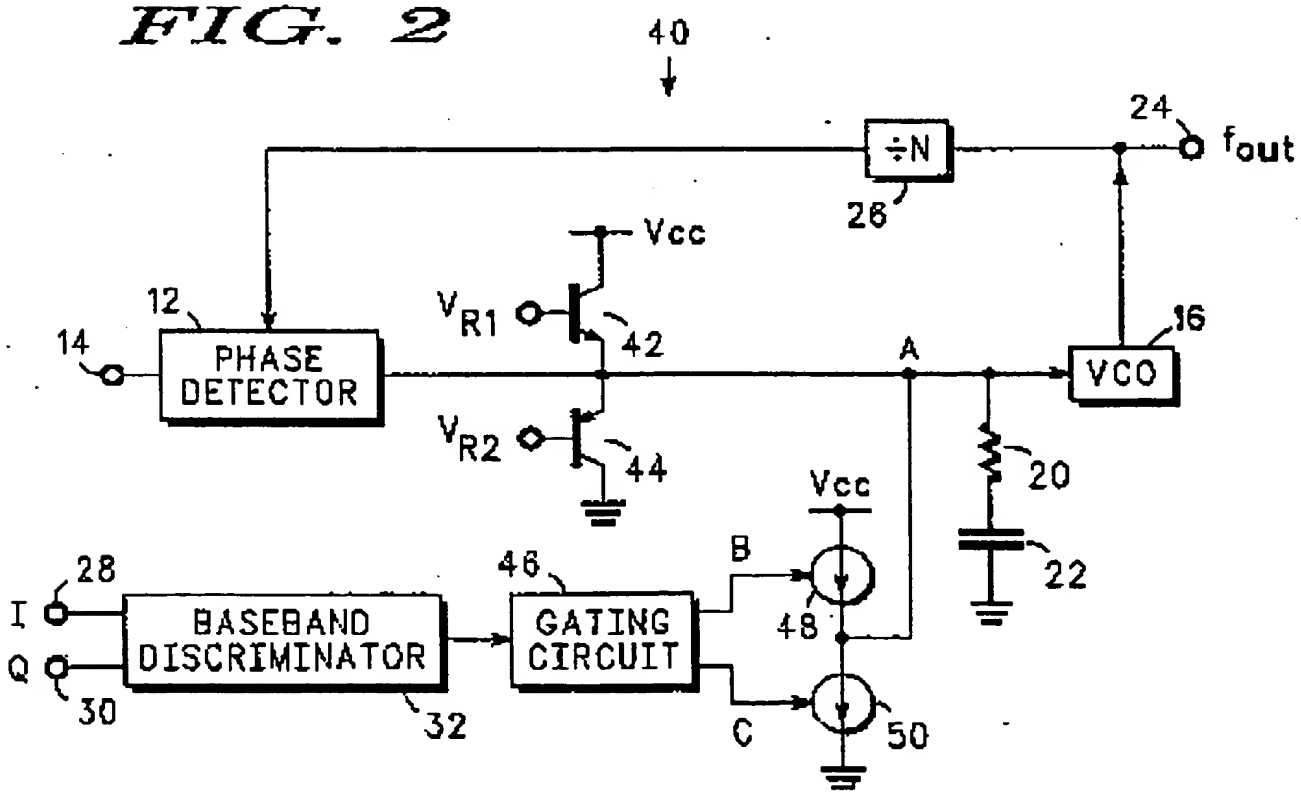


FIG. 1
-PRIOR ART-

FIG. 2



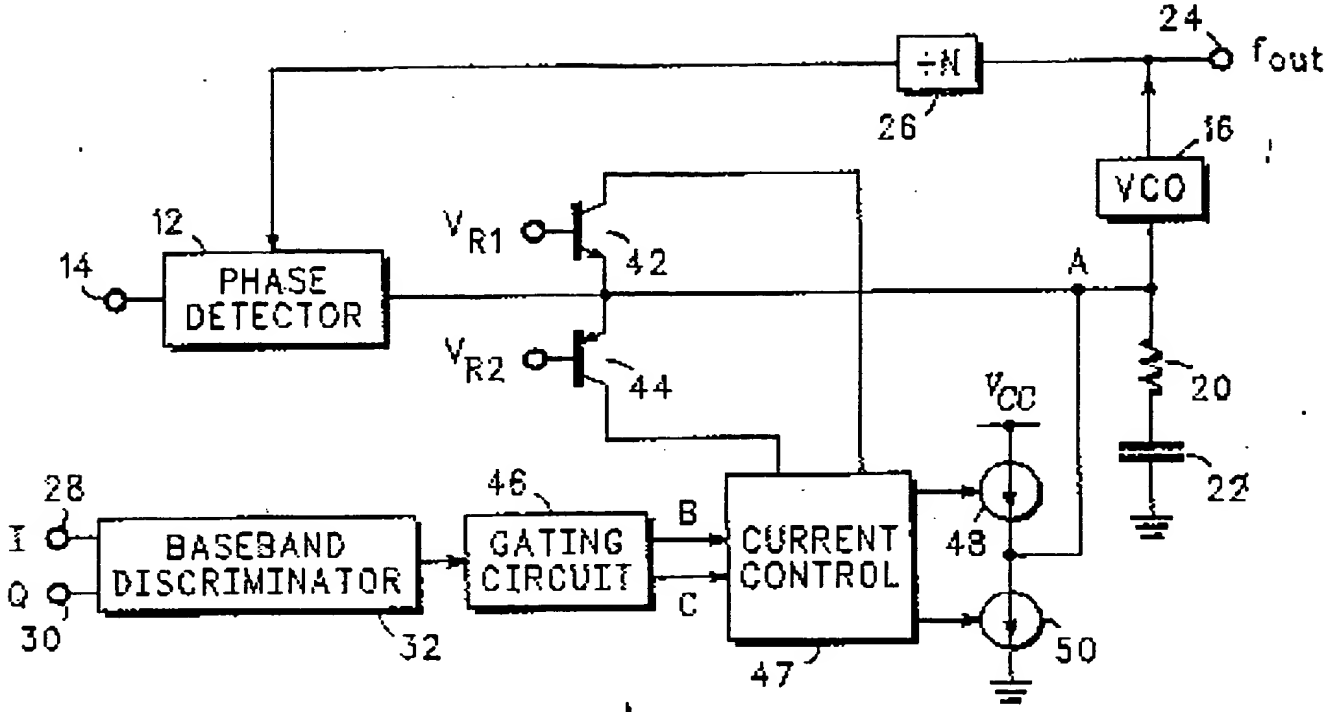
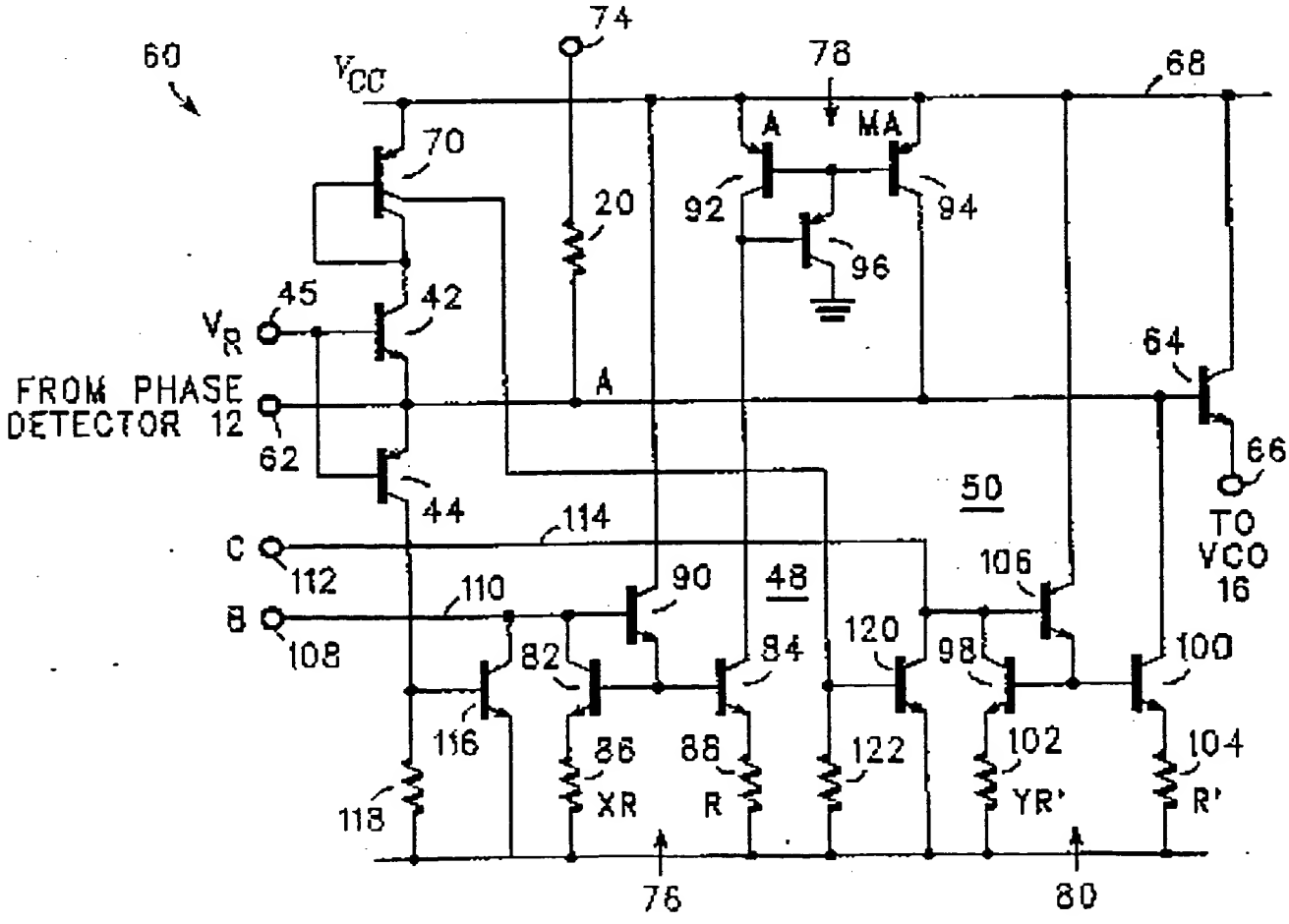


FIG. 3

FIG. 4



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(43) Date of publication of application:
09.08.89 Bulletin 89/32

(84) Designated Contracting States
DE FR GB IT

(88) Date of deferred publication of the search report:
13.06.90 Bulletin 90/24

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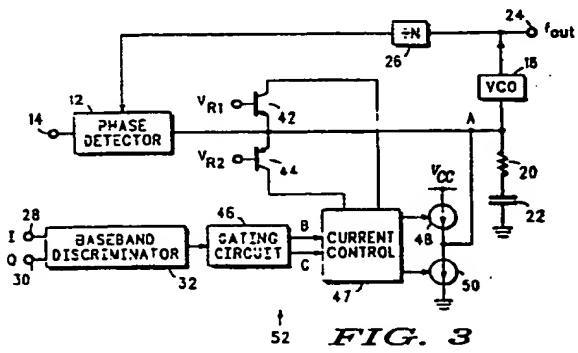

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number

EP 89 10 1330

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
P,A	US-A-4 739 284 (McGINN) * Whole document * ---	1,2,6	H 03 L 7/10
A	US-A-4 251 742 (BEELITZ) * Whole document * ---	1-5,8-10	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 14, no. 2, July 1971, page 580, New York, US; H.W. JOHNSON: "Detection and correction of phase lock failure in PLO's" ---	1,6	
P,A D	US-A-4 791 325 (McGINN) * Whole document * -----	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 03 L
H 03 K
H 04 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15-03-1990	PEETERS M.M.G.

CATEGORY OF CITED DOCUMENTS

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